A SiGe WCDMA/DCS Dual-band RF Front-end Receiver

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***Abstract* — A WCDMA/DCS dual-band RF front-end receiver IC fabricated in a 0.35-μm SiGe BiCMOS technology is presented. This RF receiver uses a novel fully-differential LNA with dual input-stages to replace the requirement of paralleling two similar LNAs in previous dual-band designs. This chip dissipates 24mA from a 2.7-V supply and can be used in direct-conversion or low-IF receiver. The measured voltage gain, P1dB and iIP3 are 32dB, -25dBm and -15dBm, respectively.**

I. INTRODUCTION

3G (Third-generation) cellular phone service has been started in Japan since 2001 and the new network will be deployed all over the world in the future years. Since the deployment speed varies between different areas, it will be convenient for cellular phone users who travel between different areas frequently if a dual-mode handset can provide both the functions of the new 3G system and the existing 2G (second-generation) system. Even after 3G deployment is finished, multi-mode handsets are still required because several 3G standards, WCDMA, cdma2000 and TD-SCDMA, will coexist all over the world. Multi-band capability is also required since different frequency bands are retained for various cellular systems. However, the multi-mode handsets will be popular only if they are comparable in size, weight, and cost with the current single-mode handset. To achieve this, one has to share as more hardware as possible between different modes and different bands.

In the RF radio, it will be a big challenge since the required specification differs from each standard. One of the critical components is low-noise amplifier (LNA). To reduce the cost of LNA, one topology is to use single wide-band LNA, which can cover several nearly bands [1]. Unfortunately, in wide-band amplifiers, a low noise figure and a high gain often come at the cost of larger power consumption. Besides, since several band-selection SAW filters are usually required for separate bands to attenuate the severe out-of-band blocking signals for a multi-band receiver, a switch may be unavoidable between the wide-band amplifier and the SAW filters otherwise the matching network at this interface becomes complicated. However, the switch increases the cost and area again and the loss of the switch also increases the total noise figure of the receiver. Nowadays, most multi-band receivers use several sets of radio-frequency circuits in parallel and each set is optimized for a certain band. Even for the PCS and DCS standards, which are only about 100MHz apart in frequency, separate narrow-band LNAs and quadrature mixers are used for performance consideration [2]. However, it increases the chip size and cost. Thus, in this paper, a WCDMA/DCS dual-band RF front-end circuit, which uses a single narrow-band LNA having dual input stages, is proposed and implemented to save chip area and cost. From the results, it is shown that the circuits can be applied to various dual-band direct-conversion or low-IF receivers around 2GHz.

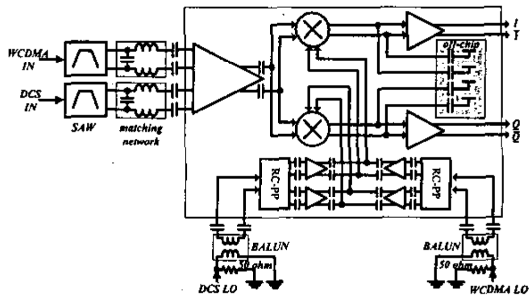

Fig. 1. Block diagram of the RF front-end receiver.

II. RECEIVER ARCHITECTURE AND CIRCUITS

A. Architecture

The down-link bands of WCDMA and DCS are 2110~2170 and 1805~1880 MHz, respectively. Fig. 1 shows the block diagram of the RF front-end receiver, which consists of a dual-band LNA, a quadrature mixer for both bands and two baseband amplifiers. The received signals are first filtered by the band-selection SAW filters. Then, one of the bands is selected to be amplified by the LNA and downconverted by the quadrature mixer. Since system-on-chip is an important trend of modern RFIC, fully-differential circuits, including the LNA, are applied to release the degradation of signal-to-noise ratio caused by the noise leakage from other noisy blocks, such as analog-to-digital converter and synthesizer. Thus, two off-chip differential matching networks are required between the LNA and the two single-ended-to-differential band-

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selection SAW filters. This IC also contains two polyphase RC filters for each band to generate the required quadrature LO signals from an off-chip LO source. The building blocks in the IC are described as follows.

B. LNA

A typical differential LNA architecture is shown in [3]. With the emitter degeneration inductors and input matching network, the base impedance of the transistor can be transformed to another impedance required by the previous band-selection filter to maximize the power transformation. Optimization of noise performance can be done simultaneously. The emitter inductors also improve the linearity of the circuit. Besides, by using inductor loads, less dc headroom is required for the load devices. Thus, the linearity of the circuit becomes better or the power supply can be reduced. Further, the load capacitance can be tuned out, and the operating frequency can be higher than a LNA using resistor loads. The main disadvantage of this LNA is the large area occupied by the four inductors. For example, a 1nH spiral inductor is about 120um X 120um in size. Besides, this LNA is narrow-band. Since the highest channel of WCDMA and the lowest channel of DCS are 365MHz apart, it is hard to apply a single narrow-band LNA to meet the required return loss and noise figure of both bands. However, if separate LNAs are used for each band, eight inductors are totally required for a dual-band design. It increases the required silicon size and product cost.

In order to save area and price, a new dual-band LNA is proposed in this design, as shown in Fig. 2. This LNA uses individual differential pair for each band (Q1-1 and Q2-1 for WCDMA, Q1-2 and Q2-2 for DCS), but the emitter inductors (L1 and L2) are shared between both bands. One of the differential pair has to be turned off at any time. For example, in WCDMA mode, "band" connects SW1 and SW2 to Vb and ground, respectively. Since SW2 will pull the bases of DCS pair to ground, all the bias current, I1, is provided to the WCDMA pair and the DCS pair is turned off. The load inductors (L3 and L4) are also shared between both bands. In WCDMA mode, "band" is low and the MOS switches, M1 and M2, are turned off. The inductors resonate with the parallel capacitors (C1 and C2) at 2.14GHz. In DCS mode, "band" is high and the MOS switches, M1 and M2, are turned on. The resonance frequency of the tank is tuned to 1.84GHz by adding two parallel capacitors (C3 and C4). In order to release the effect of process variation, parallel resistors (R3 and R4) are added to increase the bandwidth of the LNA. The two differential pairs are connected to separate band-selection filters through separate matching networks, as shown in Fig. 1. Thus, the LNA behaves like a typical

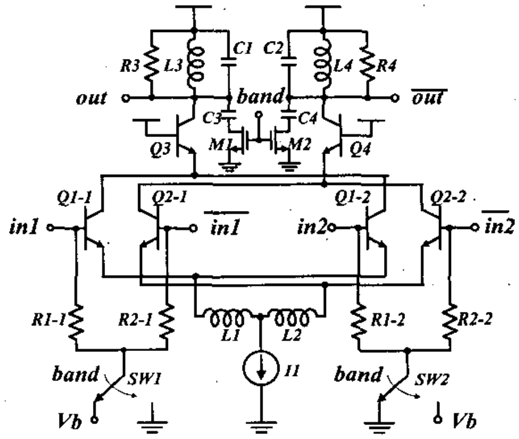

Fig. 2. Schematic of the dual-band LNA.

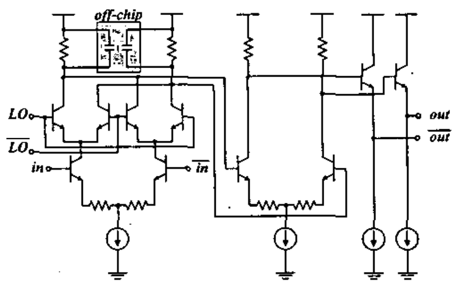

Fig. 3. Schematic of the mixer and baseband amplifier.

LNA with only small parasitic capacitors of the disabled pair added on collectors and emitters of the active differential pair. These two input stages behave like a switch, selecting signal from one of the SAW filters to be received. The SAW filter of the unselected band is isolated from the LNA. With this method, a single LNA with four inductors can be used for dual bands. Besides, it is possible to optimize each band by changing individual matching network, device size, and bias current with familiar narrow-band technique.

C. Mixer and Baseband Amplifier

Single quadrature mixer is used for both bands. Fig. 3 shows the double-balanced Gilbert-type downconversion mixer and the following baseband differential-pair amplifier of one path. Degeneration resistors are added to improve the linearity of the circuits. A 6.5 MHz low-pass pole is created by adding parallel capacitors at mixer output to relax the linearity requirement of the following baseband stages due to blocking signals. For testing convenience, out-of-chip capacitors are used. Emitter followers are used as the last stage because of the low output impedance, suitable for driving an active-RC amplifier or filter. To achieve good amplitude and phase accuracy of the quadrature LO signals, separate three-stage poly-phase filters are used for each band. In a later version of this chip, the two poly-phase filters will be replaced by one divide-by-two flip-flop to save chip areas.

III. MEASURED PERFORMANCE

The WCDMA/DCS dual-band RF front-end receiver has been fabricated in a 0.35-μm SiGe BiCMOS process. This process provides three metal layers with 3-um thick top metal and MIM capacitors. Fig. 4 shows the microphotograph of the chip. The area of the chip, including the bonding pads, is about 1550 x 1450 μm^2. The LNA occupies 520 x 470 μm^2. It means that at least an area of 520 x 470 μm^2 can be saved with the proposed LNA comparing to paralleling two similar LNAs. The chip is packaged with LQFP 32pin package and mounted on a standard FR4 printed circuit board for testing.

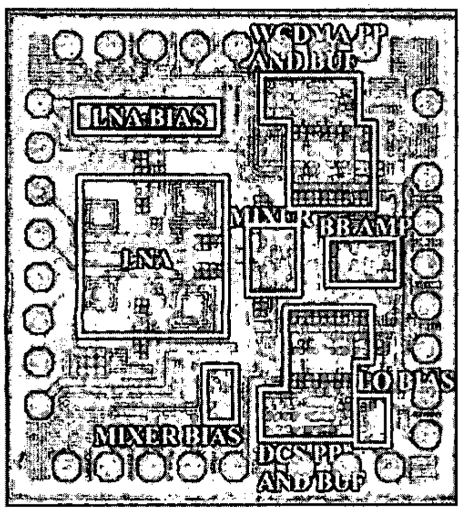

Fig. 4. Microphotograph of this chip.

The SAW filters in Fig. 1 are replaced by two baluns, whose loss is about 0.6dB, to generate the differential RF signal[4]. All of the other off-chip components, including the matching networks, have been shown in Fig. 1. Besides, -10dBm LO signals are fed into the LO baluns. The receiver is measured at the supply voltage of 2.7-V. The current dissipation of the blocks on the signal path and other measured performance are listed in Table I. The measured S_{11} is −13 and −25dB in the center of WCDMA and DCS band, respectively, as shown in Fig. 5. Fig. 6

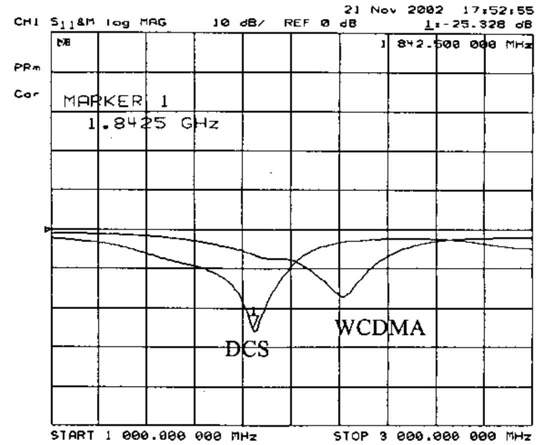

Fig. 5. Measured S_{11} of the LNA.

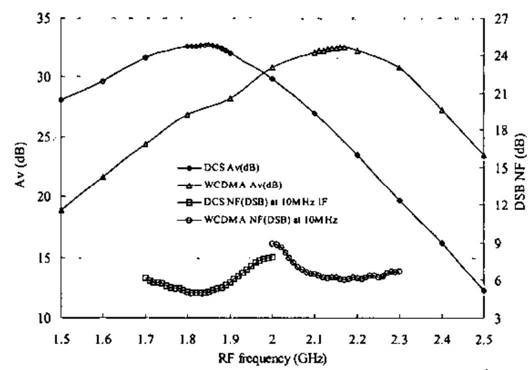

Fig. 6. Measured voltage gain and noise figure of the chip.

shows the measured voltage gain at 100kHz IF and the DSB noise figure (NF) of one single path at 10MHz IF. Voltage gain at the center of WCDMA and DCS bands is above 32dB and the measured NF at the center of both bands is 6 and 5dB, respectively. Since the balun contributes 0.6dB, the real NF of the receiver is about 5.4 and 4.4dB. The results show that the dual-band LNA can achieve the required performance of both bands with smaller chip area and convenient interface with the two SAW filters. Fig. 7 shows the linearity in WCDMA band. Similar graph can be obtained for DCS band. In WCDMA(DCS), the in-band iIP3 was measured at LO=2.14(1.8399)GHz with two tones at frequencies of 2.15(1.8408) and 2.1599(1.8416) GHz. Since WCDMA is a FDD system, in which the high power transmission signal will disturb the receiver [5], WCDMA out-of-band iIP3 was also measured at LO=2.11GHz with two tones at frequencies of 1.9799 and 2.045GHz. The WCDMA(DCS) iIP2 was measured at LO=2.14(1.84)GHz with two tones at frequencies of 2.15(1.85) and 2.1501(1.8502)GHz. The image rejection ratio (IMRR) is measured by a vector signal analyzer, HP89410, to evaluate the amplitude and phase accuracy of the quadrature mixer and baseband amplifiers [6]. Fig. 8 shows the measured IMRR of both bands, which are good enough for a typical direct-conversion or low-IF receiver.

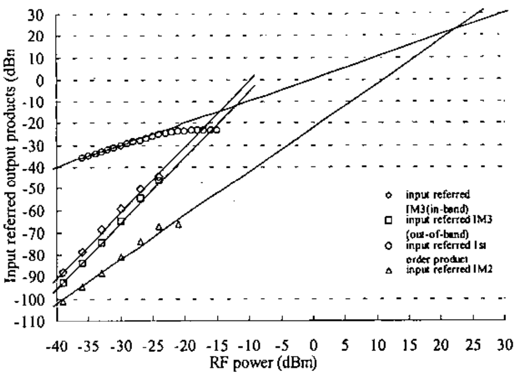

Fig. 7. Measured WCDMA linearity of the chip.

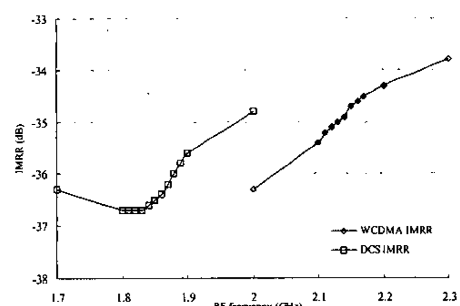

Fig. 8. Measured IMRR of the chip.

V. CONCLUSION

In this paper, a WCDMA/DCS dual-band RF front-end receiver IC fabricated in a 0.35-μm SiGe BiCMOS technology is presented. With two off-chip band-selection filters and some passive devices, it can provide a RF front-end for a WCDMA/DCS direct-conversion or low-IF receiver. This RF receiver uses a novel fully-differential LNA with dual input-stages to replace the requirement of paralleling two similar LNAs in previous design. From the measurement results, it is shown that the proposed method can be applied to two different radio bands, which are 365MHz apart. It means that the LNA can be used in dual-band receivers for various radio standards around 2GHz, such as WCDMA/cdma2000/TD-SCDMA/DCS/PCS. Multi-band application is also possible by adding more LNA input stages and finer resonance frequency tuning mechanism at the LNA output.

Table I Characteristic of Cascaded LNA and Mixer

	WCDMA	DCS
Voltage Gain	32.4dB	32.7dB
S_{11}	<-11dB	<-18dB
P1dB	-25dBm	-25dBm
In-band iIP3	-15dBm	-15dBm
Out-band iIP3	-12dBm	-
iIP2	+22dBm	+25dBm
DSB NF	5.4	4.4
IMRR	>34dB	>35dB
LNA current	8 mA @ 2.7V	
Mixer & baseband current	10 mA @ 2.7V	
LO buffer current	6 mA @ 2.7V	
Total current	24 mA @ 2.7V	
Chip area	1550μm X 1450μm	

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